A Temperature Compensation Circuit Based on Bandgap Reference

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***Abstract*—This work presents a temperature compensation circuit based in a classical bandgap reference. The circuit was designed in 0.6 µm SOI CMOS technology from X-FAB and its output presents a nonlinearity of 0.2 % as a function of the temperature. It is suitable to be used in the current preamplifier designed to enlarge the measurement capacity of Source and Measurement Units from CITAR Project.**

Keywords: CITAR, bandgap reference, SOI CMOS

I. INTRODUCTION

CITAR, acronym in Portuguese to Radiation Tolerant Integrated Circuits, is a Brazilian Project that aims the development and test of circuits and devices, which are radiation tolerant through design techniques (Radiation Hardness By Design – RHBD).

Some new devices were designed with the objective of radiation hardening such as Diamond and OCTO Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [1], [2]. These devices should be characterized after irradiation and, to do this task, it is necessary to measure the drain current I_{DS} as a function of the gate-source voltage V_{GS} for a large range of values. The device operates down to weak inversion regime, where the currents are generated by diffusion and are very small.

In order to enlarge the current measurement capacity of the Source and Measurement Units (SMUs) available to the institutions that participate of the Project, a current preamplifier was proposed [3]. Fig. 1 is an improved version of the circuit from [3]. The circuit turns the SMUs able to measure currents down to picoamperes range.

The working principle of the current preamplifier is based on the exponential relationships of voltages and currents of MOSFETs when operating in weak inversion [3]. Bipolar junction transistors (BJTs) also have this property, since the currents are generated by diffusion.

It can be proved [3] when M_0 and M_1 are in weak inversion that I_X (the unknown current) and I_M (the current to be measured) at Fig. 1 are related by the expression:

$$I_M = I_X e^{\frac{V_C}{nV_T}} \quad (1)$$

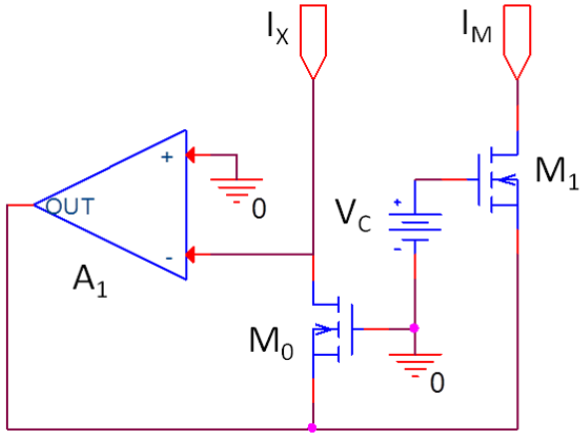

Fig. 1. Wide range current preamplifier.

In (1), V_T is the thermal voltage, which is temperature dependent and its value is 26 mV at room temperature. V_C is the voltage that controls the gain of the circuit. Because the amplification factor is an exponential term, even a small variation on V_T due to the temperature would turn to a significant error. As an example, a variation of 1 K leads to an error of 7 % in this factor. In order to compensate for the temperature effects, V_C should be also temperature dependent varying with the temperature at the same rate as V_T. Additionally, this voltage should be linear in order not to distort the gain curve with the temperature. It is expected a maximum static error in the gain of 1 dB too.

A low cost preamplifier using off-the-shelf BJTs was proposed where the amplification factor was temperature compensated [4]. However, the technologies available to the CITAR Project do not have high quality BJTs.

This work describes a circuit able to generate a temperature compensated voltage to be used in the control of the gain in the current preamplifier.

Section II describes the proposed circuit and presents the specification in order to be used in the preamplifier. Section III details the implementation of the circuit. The experimental results of the circuit output voltage as a function of the

temperature is presented in Section IV. Section V discusses the conclusions and future actions of the work.

II. The Proposed Circuit

The proposed circuit is illustrated in Fig. 2. A classical bandgap reference is formed by A1 and companion components [5]. D1, D2, R1 and R2 are dimensioned in such a way that there is a difference in the junction voltages of D1 and D2. This difference appears over R3. It can be proved [5] that the output voltage of A1 (V_{BG}) is given by:

$$V_{BG} = V_{J2} + K.V_T \quad (2)$$

where V_{J2} is the voltage drop at the junction of D_2, V_T is the thermal voltage and K is a constant given by:

$$K = \frac{R_2}{R_3} V_T \ln \frac{R_2 I_{S2}}{R_1 I_{S1}} \quad (3)$$

where I_{S1} and I_{S2} are the reverse currents of D1 and D2 respectively.

Since V_{J2} has a negative coefficient with relation to the temperature and V_T a positive one, K can be adjusted in order V_{BG} should have positive or negative net thermal coefficient.

Since V_T is specified to the temperature of 27 °C (300 K), V_C should be also calculated to this temperature. Considering a thermal rate of the bandgap reference at Fig. 2 of 2 mV/K, at 300 K *Vout* should be 600 mV. This way, this voltage compensates for the variation of V_T with temperature in the exponent of the current preamplifier amplification factor. V_C in Fig. 1 is obtained thru a resistive divider from *Vout*. The use of smaller thermal rates turn the circuit more sensitive to the thermal rates of the other components and more difficult to adjust.

In order to accomplish these specifications, A2 and the remaining components were introduced, aiming to compensate for process variations. The first step is, at 27 °C (300 K), to adjust R5 to have 600 mV in the positive terminal of A2.

Further step is the adjustment of R9 in order *Vout* is also 600 mV. Since A2 is in the linear operation, the negative terminal has also 600 mV due to the adjustment of R5 and then no current flows through R6 and R7. *Vout* is centered in 600 mV and any change should be caused exclusively by the influence of the temperature in V_{BG}. The thermal coefficient of the complete circuit is modified through R7. This potentiometer changes the gain of the non-inverter amplifier made with A2 and thus the variation of *Vout* with the temperature. To adjust the thermal coefficient, the circuit should be at a different temperature, fitting *Vout* to the expected voltage to that temperature.

R3 enables an additional degree of adjustment of the thermal coefficient of the circuit.

III. Circuit Implementation

The circuit was produced in 0.6 µm SOI CMOS technology (XT06) from X-FAB. The photography of the chip is seen in Fig. 3. In order to obey the design rules and due to their special connections, D1 and D2 were constructed with a trench surrounding them. The chip has dimensions of 156 µm x 306 µm.

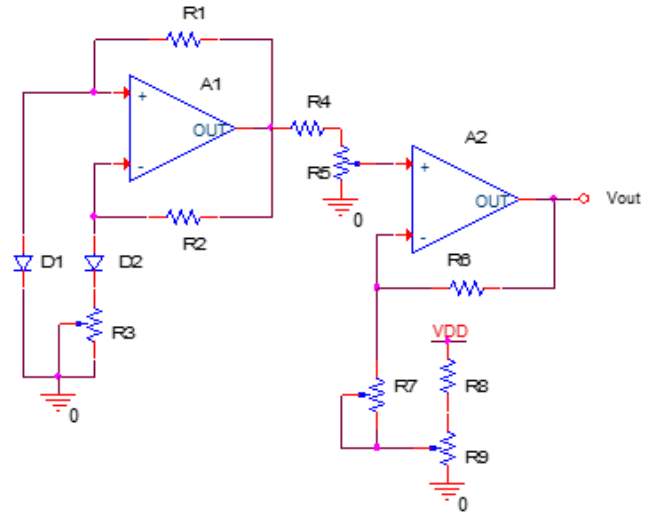

Fig. 2. Temperature compensation circuit.

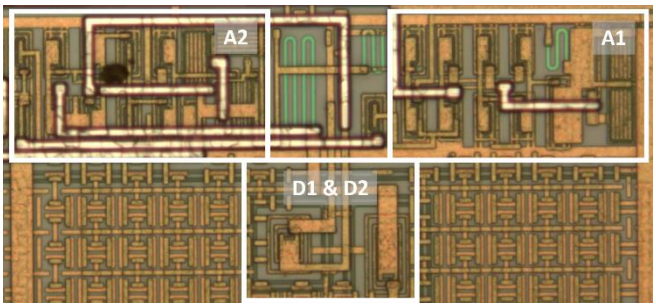

Fig. 3. Layout of the temperature compensation circuit.

The detailed schematic diagram from Cadence is illustrated in Fig. 4. In some works, the diodes are obtained through the parasitic pnp BJT in the CMOS process [5]. In this work, D1 and D2, at the center of Fig. 3, correspond to the junction of the substrate and the n+ diffusion layer at the drain and source regions of MOSFETs. It is expected they have the same thermal coefficients of junction diodes, i.e., about -2 mV/K.

Op-amps have two stages, where the gain of the second stage is increased using both inverting and non-inverting outputs from input differential pair. An external resistor and a diode-connected transistor defines the bias current. With a resistor of 1 MΩ the bias current is 10 µA.

IV. Experimental Results

The behavior of the circuit was investigated as a function of the temperature using a SM8200 Thermotron climatic chamber. The circuit is powered by an Agilent E3631A triple output power supply with 5 V and 0 V. The output voltage is measured using a Fluke 17B+ digital multimeter.

The thermal behavior of the circuit is evaluated in the range of 20 °C to 40 °C, since it is aimed to be used in lab environment. At first, the chamber is programmed to 27 °C without humidity control. R5 and R9 are then adjusted as explained in the last Section. With the chamber programmed to 40 °C and after stabilization, R7 is adjusted in order *Vout* be 626 mV.

R3, R5, R7 and R9 are 20 kΩ, 100 kΩ, 100 kΩ and 1 kΩ potentiometers respectively. R8 is a 3.9 kΩ fixed resistor. Remaining resistors belong to the chip.

The temperature is adjusted in steps of 2 °C from 40 °C down to 20 °C with *Vout* recorded for each temperature. The final graph is shown in Fig. 5. The circuit has a nonlinearity of 0.2 %, a thermal coefficient of 2.35 mV/K and a shift from 600 mV at 27 °C of 4 mV. The deviation in the thermal rate causes an error at the gain of 20 %. The static error of the gain is less than 1 dB.

V. Conclusions and Future Works

The circuit presents high linearity with temperature. However, the adjustment of the voltage at 27 °C is quite sensitive, since it is expected a resolution of 1 mV at an output of 600 mV. The same is noted in the gain adjustment. It is believed that, using more appropriate values of resistance, the curve can be fitted to the ideal one. For this task, it is necessary to assemble and repeat the tests with more samples.

Acknowledgment

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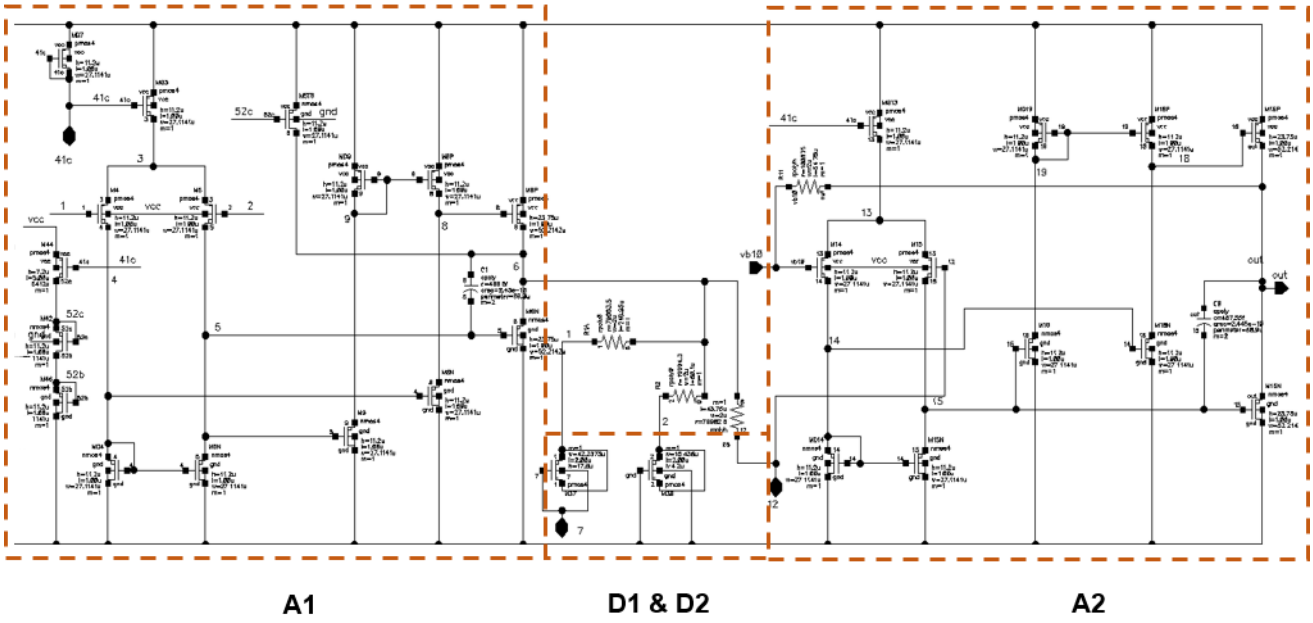

Fig. 4. Schematic diagram of the temperature compensation circuit.

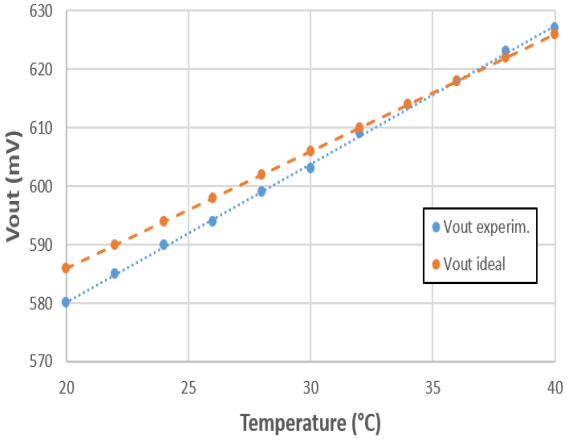

Fig. 5. Output voltage of the circuit as a function of the temperature.

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